REMARKS/ARGUMENTS

Claims 1-10, 17, and 18 are pending in this application. By this Amendment, Applicant AMENDS the specification and ADDS Drawing Fig. 14.

Applicant's undersigned attorney hereby declares that no new matter has been added by new Fig. 14, and that the subject matter shown in new Fig. 14 was described in the originally filed application.

The Examiner objected to claims 3, 8, 17, and 18 for allegedly containing minor informalities. Applicant has added Fig. 14 to correct the minor informalities in claims 3 and 8 noted by the Examiner. The Examiner is reminded that the shorthand notation used by Applicant in claims 17 and 18 is well accepted practice before the U.S. Patent & Trademark Office. See MPEP § 2173.05(f); Ex parte Porter, 25 USPQ2d 1144 (Bd. Pat. App. & Inter. 1992); and Ex parte Moelands, 4 USPQ2d 1474 (Bd. Pat. App. & Inter. 1987). Accordingly, Applicant respectfully requests reconsideration and withdrawal of the objection to claims 3, 8, 17, and 18.

Claims 1, 4, 5, 6, 9, and 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ferrant (US Patent 6,556,092). Applicant respectfully traverses the rejection of claims 1, 4, 5, 6, 9, and 10.

Claim 1 recites:

> "An oscillator device comprising:
> **an oscillation circuit including an NPN oscillation transistor and a buffer amplifier circuit including a PNP buffer amplifier transistor**; wherein
> the NPN oscillation transistor and the PNP buffer amplifier transistor are connected in series to a power supply;
> a collector of the NPN oscillation transistor is connected to a power terminal and is grounded via a capacitor;
> **a base of the PNP buffer amplifier transistor is grounded via a capacitor**;
> at least one of a resistor and an inductor is connected between a collector of the PNP buffer amplifier transistor and the ground;
> the collector of the PNP buffer amplifier transistor is AC-connected to an output terminal; and

an emitter of the NPN oscillation transistor and an emitter of the PNP buffer amplifier transistor are directly connected." (Emphasis added)

Claim 6 recites features that are similar to the features recited in claim 1, including the above-emphasized features.

Applicant agrees that Ferrant fails to teach or suggest a capacitor connected between the power terminal Vdd and the ground, the buffer (MN1) is AC-connected to the output, and the complementary pair of bipolar transistors. The Examiner alleged in the first full paragraph on page 3 of the outstanding Office Action "it is old and well known in the art that the bipolar transistors and the FET transistors are exchangeable and bipolar transistors are faster than FET transistors; a capacitor that is coupled between the power terminal and the ground will ground the power terminal at high frequencies and the AC coupling capacitor is used for blocking the direct current." Thus, the Examiner concluded that it would have been obvious "to couple a capacitor between the power terminal (Vdd) and the ground of the power terminal to ground the power terminal at high frequencies, to incorporate a capacitor to the output terminal to block the direct current and to replace the complementary pair of complementary FET transistor[s] (MN1, MP1) of Ferrant with a pair of complementary bipolar transistors for having better switching speed at high frequencies."

The Examiner is reminded that prior art rejections must be based on evidence. Graham v. John Deere Co., 383 U.S. 117 (1966). The Examiner has failed to establish a *prima facie* case of obviousness of the claimed invention because all of the claimed features must be taught or suggested by the prior art. Since the Examiner has completely failed to provide any reference which teaches or suggests the features of "an oscillation circuit including an NPN oscillation transistor and a buffer amplifier circuit including a PNP buffer amplifier transistor" and "a base of the PNP buffer amplifier transistor is grounded via a capacitor," the Examiner has clearly failed to establish a *prima facie* case of obviousness. See In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974) and MPEP § 706.02(j) and § 2143.03.

Further, even assuming *arguendo* that the prior art teaches all of the features alleged by the Examiner, the Examiner has only provided conclusions and has not provided any motivation or suggestion for modifying Ferrant. That is, the Examiner has completely failed to explain why the circuit in Ferrant (1) requires faster switching times; (2) requires blocking the direct current at the output terminal; or (3) requires the power terminal be grounded at high frequencies. Thus, the Examiner has also failed to establish a *prima facie* case of obviousness because he has failed to offer any suggestion or motivation for modifying Ferrant. See In re Nielson, 816 F.2d 1567, 2 USPQ 2d 1525, 1528 (Fed. Cir. 1987).

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 1 and 6 under 35 U.S.C. § 103(a) as being unpatentable over Ferrant.

Accordingly, Applicant respectfully submits that none of the prior art of record, applied alone or in combination, teaches or suggests the unique combination and arrangement of elements recited in claims 1 and 6 of the present application. Claims 2--5, 7-10, 17, and 18 depend upon claims 1 and 6 and are therefore allowable for at least the reasons that claims 1 and 6 are allowable.

In view of the foregoing amendments and remarks, Applicants respectfully submit that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

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